ADSP-2181 EZ-KIT Lite
Evaluation System Manual

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1 INTRODUCTION

Thank you for purchasing the ADSP-2181 EZ-KIT Lite™ evaluation kit. The evaluation board is designed to be used in conjunction with VisualDSP++™ and the 16-bit tools as a complete code evaluation and debug system. This product is shipped with the VisualDSP++ integrated development environment, which contains the code generation tools (C compiler, linker, and assembler). Using the EZ-KIT Lite with the debugger, you can observe the ADSP-2181DSP execute programs from on-chip RAM, interact with on-board devices, and communicate with other peripherals located on optional add-on modules.

You can access the ADSP-2181 processor from a PC through a serial port or an optional emulator. The monitor program gives you complete target debug capability through the serial port. In contrast, the emulator allows the PC to perform in-circuit emulation through the processor's emulation port.

The board's features include:

- ADSP-2181, 33 MIPS DSP
- AD1847 stereo codec
- RS-232 interface
- Socketed EPROM
- User pushbuttons
- Power supply regulation
- Expansion connectors
- User configurable jumper

The EZ-KIT Lite board is equipped with hardware that facilitates interactive demonstrations. Pushbutton switches and user programmable LEDs provide user control and board status. Additionally, the AD1847 SoundPort codec provides access to an audio input (selectable as line level or microphone) and an audio output (line level).

The EZ-KIT Lite includes a monitor program stored in the socketed EPROM. The monitor program lets the board communicate over the serial port to a PC. This monitor program lets you download, execute, and debug ADSP-2181 programs.

You can also connect an EZ-ICE® (in-circuit emulator) to the EZ-KIT Lite. Through the EZ-ICE, you can load programs, start and stop program execution, observe and alter registers and memory, and perform other debugging operations. The EZ-ICE emulator is available from Analog Devices.

Additionally, the EZ-KIT Lite provides user installed expansion connectors that let you examine processor signals, as well as provide an interface for host control.

1.1 For More Information About Analog Devices Products

Analog Devices is accessible on the Internet at www.analog.com. The DSP Web page is directly accessible at www.analog.com/dsp. This page provides access to DSP specific technical information and documentation, product overviews, and product announcements.

1.2 For Technical or Customer Support

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- Fill out the Tech Support form located on the Analog Devices web site: www.analog.com/technology/dsp/contactUs.html
- Email questions to dsptools.support@analog.com
- Contact your local Analog Devices sales office or an authorized Analog Devices distributor

1.3 Purpose of This Manual

The ADSP-2181 EZ-KIT Lite evaluation system manual gives directions for installing the board and software, and using the demonstration programs on your PC. Also, this manual provides guidelines for running your own code on the ADSP-2181 DSP.

1.4 Intended Audience

This manual is a user's guide and reference to the ADSP-2181 EZ-KIT Lite evaluation board. DSP programmers who are familiar with Analog Devices 16-bit DSP architecture, operation and programming are the primary audience for this manual.

DSP programmers who are unfamiliar with Analog Devices DSPs can use this manual, but should supplement this manual with the appropriate processor User's Manual and the VisualDSP++ tools manuals.

1.5 Manual Contents Description

This manual contains the following information:

- Chapter 2 — Getting Started

  Provides software and hardware installation procedures, PC system requirements, and basic board information.

- Chapter 3 — Using EZ-KIT Lite software

  Provides information on the EZ-KIT Lite system from a software perspective, and details the monitor program and codec.

- Chapter 4 — Demonstration Programs

Provides information on the demonstration programs that ship with your EZ-KIT Lite and VisualDSP++ Debugger reference information.

- Chapter 5 — Working With EZ-KIT Lite Hardware

  Provides information on the hardware aspects of the evaluation system and on the connectors to the ADSP-2181 interface and AD1847 pins.

- Appendix A — Restrictions

  Provides information on board restrictions you may encounter when using your EZ-KIT Lite evaluation system.

- Appendix B — Bill of Materials

  Provides a list of components used in the manufacture of the EZ-KIT Lite board.

- Appendix C — Schematics

1.6 Documentation and Related Products

For more information on the ADSP-2181 and the components of the EZ-KIT Lite system, see the following documents:

- *ADSP-218x-DSP Instruction Set Reference*
- *ADSP-218x-DSP Hardware Reference*

The ADSP-218x family of processors is supported by a complete set of development tools. Software tools include a C compiler, assembler, runtime libraries and librarian, linker, simulator, and PROM splitter. These tools are described in the following texts:

- *VisualDSP++ Getting Started Guide for ADSP-21xx DSPs*
- *VisualDSP++ User's Guide for ADSP-21xx DSPs*
- *VisualDSP++ C/C++ Compiler and Library Manual for ADSP-218x DSPs*
- *VisualDSP++ Linker and Utilities Manual for ADSP-21xx DSPs*
- *VisualDSP++ Assembler and Preprocessor Manual for ADSP-21xx DSPs*
- *VisualDSP++ Product Bulletin for ADSP-21xx DSPs*

These documents are found on the Analog Devices' Technical Documentation web site at: www.analog.com/library/dspManuals/16BitIndex.html

If you plan to use the EZ-KIT Lite in conjunction with the EZ-ICE emulator, refer to the documentation that accompanies that product.

1.7 Conventions

The following conventions are used throughout this manual:

- The ⃠ graphic indicates restrictions and warnings.
- The ⓘ graphic indicates important information.

2 GETTING STARTED

2.1 Overview

This chapter provides you with the information you need to install your software and the ADSP-2181 evaluation board. It is important that you install your software and hardware in the order presented for correct operation.

2.2 Contents of Your EZ-KIT Lite Package

The EZ-KIT Lite evaluation board contains ESD (electrostatic discharge) sensitive devices. Electrostatic charges readily accumulate on the human body and equipment and can discharge without detection. Permanent damage may occur on devices subjected to high energy discharges. Proper ESD precautions are recommended to avoid performance degradation or loss of functionality. Unused EZ-KIT Lites should be stored in the protective shipping package.

Your ADSP-2181 EZ-KIT Lite evaluation package contains the following items. If any item is missing, contact the vendor where you purchased your EZ-KIT Lite or Analog Devices.

- ADSP-2181 EZ-KIT Lite board
- Power cable with 8-10V DC power supply
- RS-232 serial port 9-pin cable
- One CD-ROM containing the VisualDSP++ software and EZ-KIT Lite software with examples.

2.3 Installation Procedures

The following procedures are provided for the safe and effective use of the ADSP-2181 evaluation board. It is important that you follow these instructions in the order presented to ensure correct operation of your software and hardware. After you have completed the physical set up of your board, you can load and run the demonstration programs contained on the distribution media. For more information, see Chapter 4 Demonstration Programs.

2.3.1 Installing the EZ-KIT Lite Board

The ADSP-2181 EZ-KIT Lite board is designed to run outside your personal computer as a stand-alone unit. You do not have to remove the chassis from your computer. Use the following steps to connect the EZ-KIT Lite board:

1. Remove the EZ-KIT Lite board from the package—be careful when handling the board to avoid the discharge of static electricity, which may damage some components.

2. Connect the RS-232 cable to an available Comm Port on the PC and to J3 on the ADSP-2181 evaluation board.

3. Plug the provided cord into a 120-Volt AC receptacle and plug the connector at the other end of the cable into J4 on the evaluation board.

All of the LEDs light up briefly. The power (green) LED remains on and FL1 blinks. If the LED does not light up, check the power connections.

To configure your board to take advantage of the audio capabilities of the demos, use the following procedure:

1. Plug a set of self-powered computer speakers into jack J1 on the board. Turn on the speakers and set the volume to an adequate level.

2. Connect the line out of an electronic audio device to jack J2 on the board. Set jumper JP2 to LINE.

3. Open Jumper JP2 to GND to enable the AD1847 codec. (This is the board default).

This completes the hardware installation. For complete information on the EZ-KIT Lite board, see "Board Layout".

2.3.2 Installing VisualDSP++

Your EZ-KIT Lite comes with the latest version of VisualDSP++ for the ADSP-21xx DSPs. You must install this software prior to installing the EZ-KIT Lite software.

2.3.2.1 System Requirements

Verify your PC has the minimum requirements.

Table 2-1 System Requirements

Windows® 98, ME, 2000, XP	Windows NT™
Windows 98, ME, 2000, XP	Windows NT 4.0, Service Pack 3 or later
Pentium processor 166MHz or faster	Pentium processor 166MHz or faster
100 MB available space	100 MB available space
16 MB RAM	16 MB RAM
VGA Monitor and color video card	VGA Monitor and color video card
CD-ROM	CD-ROM

2.3.2.2 To Install the Software

1. From the initial screen, select VisualDSP++ Installation.
2. Respond to the installation dialog screens.

2.3.2.3 To Install the License

You need to supply the serial number provided on the sticker affixed to the CD case.

1. From the initial screen, select Install License.
2. Select single user license.
3. Respond to the installation dialogs.

This installs a permanent limited license.

This limited license, lets you run EZ-KIT Lite sessions only. Simulation and emulation are not supported. For a full license, contact your local Analog Devices sales representative.

2.3.2.4 To Register the Product

You can fax your registration card to (603) 882-2655 or mail to:

Attn: Registration
Analog Devices, Inc.
20 Cotton Rd
Nashua NH, 03063

Please note that the VisualDSP++ software that comes with your EZ-KIT Lite is a demo version that limits executable file size to 8K bytes. The EZ-KIT Lite board is also the only target you can attach to. You may upgrade your license by contacting your local Analog Devices sales representative.

2.3.2.5 To View the Documentation

To view documentation on-line, you must have a .pdf reader installed. The Adobe® Acrobat® installation kit has been included on the CD-ROM for your convenience. To install Adobe Acrobat Reader, click Adobe Acrobat Reader in the initial screen and respond to the dialog boxes as prompted.

2.3.3 Installing the EZ-KIT Lite Software

The EZ-KIT Lite utility software is supplied the same CD as VisualDSP++, please follow these steps:

1. Close VisualDSP++ and all Windows applications.

   You cannot install any of the EZ-KIT Lite software if any VisualDSP++ applications are running. You should close all Windows applications also.

2. Install the EZ-KIT Lite software by responding to the installation dialog screens.

2.3.3.1 Default Settings

After you have installed the board and utility software, your PC and EZ-KIT Lite have the default settings shown in Table 2-2. You can change these settings in the dialog box that pops up the first time you start VisualDSP++.

Table 2-2 User Configurable EZ-KIT Lite Settings

Selection	Default Setting
Comm Port	Comm 1
Baud Rate	9600

3 USING EZ-KIT LITE SOFTWARE

3.1 Overview

The combination of the EZ-KIT Lite board and the monitor software operate as a target for the VisualDSP++ debugger. The debugger lets you view processor registers and memory and perform several debugging activities, such as setting breakpoints, stepping through code, and plotting a range of memory.

3.2 Standard Operation

This section covers the standard operation of the EZ-KIT Lite board. It describes the I/O capabilities of the on-board components, board power-up, and the on-board monitor program.

3.2.1 I/O Devices

3.2.1.1 Flags

The ADSP-2181 has one asynchronous FLAG I/O pin. The FL1 Pin is connected to the red FL1 LED. This lets you visually inspect states of your program.

3.2.1.2 Interrupts

The ADSP-2181 EZ-KIT Lite has one external interrupt connected through pushbutton switch S2. This corresponds to external interrupt IRQE.

The external interrupts are controlled through the ICNTL and IMASK registers and are configured by modifying the interrupt vector table or through instructions in user code. The ICNTL register also controls the interrupt sensitivity between level and edge. To prevent an interrupt from being masked, write to the IMASK register.

The monitor program running on the ADSP-2181 uses one interrupt (the timer) for normal operation. When downloading your own code through the monitor program, the timer interrupt vector is protected and cannot be overwritten. If these vectors are overwritten, or the timer interrupt is masked in any way, the debugger will not be able to communicate with the host program. The following rules and restrictions should be followed when using interrupts:

- Do not step into an interrupt.
- Interrupts are disabled when the user program is halted.

- The board cannot communicate with the host if interrupt nesting is enabled.
- If you do not require the supplied monitor program, a start-up routine that dynamically alters the timer interrupt vector can be used. This removes all monitor functionality.

3.2.1.3 Serial Ports

The ADSP-2181 features two synchronous bi-directional Serial Ports (SPORTs). The SPORTs can operate at up to 1x clock frequency, providing each with a maximum data rate of 30 Mbit/sec. SPORT data can be automatically transferred to and from on-chip memory using DMA.

SPORT0 is connected to the on-board AD1847. The CODECDIS signal available on connector P3 can be used to disable the codec. When this signal is brought low, the codec is disabled and its signals are put in a high impedance state. SPORT1 is connected to the RS-232 interface and is used as a software UART. Communications between the monitor and the host are through SPORT1.

For more information on the Serial Ports, refer to your processor's User's Manual.

3.2.2 POST Routines

POST (Power On Self-Test) routines are a series of standard tests and initializations that the EZ-KIT Lite performs on a power-on reset. To perform a power-on reset, disconnect power to the board for at least three seconds and then reconnect power. The board automatically resets (note that all the LEDs light up briefly). You may also reset the board during operation through the Debug Reset command in the debugger. Both types of reset cause the DSP to reset to a known state. At this point you should reload any programs you were working on. Table 3-1 shows the types of resets and their functions

Table 3-1 Post Routines

Routine	Power-on Reset	Reset During Operation
EPROM Load	Yes	No
AD1847 Check	Yes	No
Initializations	Yes	Yes

3.2.2.1 Memory Checks

The monitor program performs these standard memory checks:

1. EPROM
2. Internal RAM

The EPROM test consists of verifying a number in memory. If the monitor code is corrupted, the monitor may crash before reaching the actual program code.

3.2.2.2 UART Check/Initialization

The software UART check is performed when it attempts to connect to the EZ-KIT Lite through a Transmitted Loop Back routine. This UART test is performed by the host after the POST is complete. In this test, the host sends the UART test protocol. This protocol specifies the number of bytes that are transmitted to the EZ-KIT Lite board, and instructs the board to echo the byte stream back to the host. This test determines whether the EZ-KIT Lite board is set to the correct baud rate, and verifies the external connections between the board and the host.

On power up, the EZ-KIT Lite board defaults to a baud rate of 9600 with 8 data bits, 1 stop bit, and no parity. To change this rate, wait for the POST routine to complete and then use the Settings Baud Rate command in the debugger. Note that setting the baud rate to a lower number can significantly slow the board's response to all debug activities.

Different baud rates should be selected based on the type of code you are working with. For real-time interrupt driven programs, a lower baud rate setting slows performance but the timer interrupt occurs less frequently. This gives your program a larger share of the processors resources.

3.2.2.3 AD1847 Check/Initialization

On reset, the AD1847 is inactive. An initialization routine initializes the codec by sending a series of command words through the SPORT0 TX interrupt. Once the commands have been sent and the AD1847 is initialized, it begins transmitting the clock which synchronizes data transfers to and from the DSP. Once this bit goes high, the AD1847 is ready for standard communication over SPORT0.

3.2.3 Monitor Program Operation

The monitor program runs on the EZ-KIT Lite board as part of the DSP executable, and provides the ability to download, debug, and run user programs. The VisualDSP++ debugger is the interface to the monitor. Using the EZ-KIT Lite as a target with the debugger lets you operate the board remotely.

There are three main components of the monitor program:

- Halt loop
- UART ISR (Timer ISR)
- Command Processing Kernel

The monitor program idles in the halt loop when it is not running user code. While there, you can read/write memory, read/write registers, download programs, set breakpoints, change the UART's baud rate, and single-step through code. To enter the halt loop from your code, you must suspend or stop user code—either with a breakpoint or a halt instruction. At this point, the halt loop polls the UART. With every character received from the UART, the command-processing kernel

verifies whether a full command has been received. If a command has been received, the kernel processes the command; otherwise, control is returned to the halt loop to wait for more characters. The only method of executing your code once the halt loop has been entered is to send a Run or Single-step command from the debugger.

The UART ISR is entered when your code is running, but the host is still interacting with the board. As the host sends bytes, the UART ISR takes the data stream from the UART, and builds the command. As with the halt loop, each character received is passed to the command-processing kernel. Unlike the halt loop, the monitor returns to your code immediately after the interrupt is serviced.

The following restrictions should be followed to ensure correct board operation.

- The host loses contact with the monitor while the user program is running if the user program disables the Timer interrupt or changes the Timer interrupt vector.
- The host loses contact with the monitor while the program is running, and it enters an Interrupt Service Routine when nesting is turned on.
- The host cannot halt with the debugger's Debug Halt command if global IRQ enable is disabled. However, breakpoints will work.
- The debugger will have trouble halting at a baud rate over 9600 while using the monitor program.

Command processing, initiated from either the UART ISR or the halt Loop, is done in the command-processing kernel. This kernel parses the commands and executes the instructions. If the instruction requires data to be sent back to the host, the kernel initiates the response.

3.2.3.1 Breakpoints

The ability to stop the execution of code and examine processor registers and memory is extremely helpful when debugging code. Note that the debugger automatically inserts breakpoints at the function Main(), when the Settings Run To Main command is selected, and at _exit instruction.

3.2.4 AD1847 Transmissions

After initialization, the AD1847 generates the clock used to transfer data across SPORT0. The ADSP-2181 initiates all transmissions with the AD1847 by sending a synchronization pulse. Even though the AD1847 transmits the data clock, it may not be ready for normal operation.

Initialization of the AD1847 is performed by sending 13 control words contained in a circular buffer to the AD1847. This is usually done via the SPORT0 TX interrupt routine. Once the codec is initialized, autobuffering is used to fill up the TX and RX buffers, which use circular buffering. Once the circular buffer wraps around, then either a TX or RX interrupt occurs. Then the DSP will process the interrupt request.

3.3 Running Your Own Programs

This section provides the basic information you need to run your own programs on the ADSP-2181 EZ-KIT Lite. You build these programs using the 16-bit tools. This information includes rules for using processor memory and a simple program generation procedure.

Although there are many ways to go about developing programs in the VisualDSP++ environment, all program development within the environment should include the following steps:

- Step 1: Create a New Project File
- Step 2: Set Target Processor Project Options
- Step 3: Add and Edit Project Source Files
- Step 4: Customize Project Build Options
- Step 5: Build a Debug Version of the Project
- Step 6: Debug the Project
- Step 7: Build a Release Version of the Project

By following these steps, your DSP projects build consistently and accurately with minimal project management. Note the following restrictions of this system:

⃠ The size of the DSP executable that you can build using the EZ-KIT Lite tools is limited to 8K.

⃠ Do not run more than one ADSP-2181 EZ-KIT Lite session in the debugger at any one time. You may run an EZ-KIT Lite session and a simulator or ICE session at the same time, or you can open two debugger interfaces to run more than one EZ-KIT Lite session.

3.3.1 ADSP-2181 Memory Map

The ADSP-2181 EZ-KIT Lite board contains 80K bytes configured as 16K x 24 program memory and 16K x 16 of internal SRAM that can be used for program or data storage. The configuration of on-chip SRAM is detailed in the ADSP-2181 data sheet. Table 3-2 shows the memory map of the ADSP-2181 EZ-KIT Lite.

Table 3-2 Memory Map

Start Address	End Address	Content
PM 0x0000	0x002F	Interrupt vector table
PM 0x0030	0x17CF	Available for user code
PM 0x17D0	0x1FFF	Reserved for monitor code
PM 0x2000	0x3FFF	Available for user code
DM 0x0000	0x3AFF	Available for user data
DM 0x3E00	0x3FFF	Available for user data
DM 0x3B00	0x3DFF	Reserved for monitor data

3.3.2 Using the AD1847 Dual-Analog Front End

The monitor does not initialize the AD1847. This provides you with greater flexibility to experiment with custom codec operations. Simple programs such as Echo are provided with your EZ-KIT Lite which show basic codec operation. It is recommended that you model your code using these examples.

4 DEMONSTRATION PROGRAMS

4.1 Overview

This chapter describes loading and running the demonstration programs supplied with the ADSP-2181 EZ-KIT Lite board. The demos are designed to run on the VisualDSP++ debugger which is supplied on the CD-ROM that shipped with this product. For detailed information on debugger features and operation, see the *VisualDSP++ User's Guide for ADSP-21xx Family DSPs* and VisualDSP++ Online Help.

4.2 Starting the VisualDSP++ Debugger

After the VisualDSP++ software and license have been installed, click the Windows Start menu.

1. Select Programs/VisualDSP/VisualDSP++ Environment from the Start menu.

   The debugger interface appears.

2. From the Session menu, select New Session.

   The Target Selection dialog box appears.

3. Configure the debug session as shown in Figure 4-1and click OK.

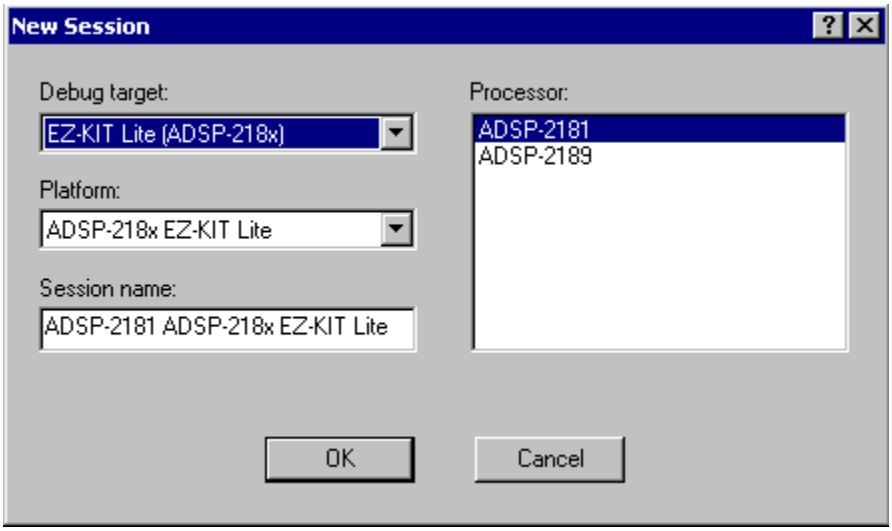


Figure 4-1 Target Selection Dialog Box

A Target Message appears.

Figure 4-2 Target Message

4. Press the Reset button on the evaluation board.

   All the LEDs light up and after a brief delay (< 2 seconds), FL1 will then blink and the PWR LED will stay lit.

   During this delay, the POST tests run to verify operation of the AD1847 and the EPROM.

5. Click OK.

   The initialization completes and the Disassembly window opens. The code in the Disassembly window is the EZ-KIT Lite monitor program.

4.2.1 Debugger Operation with the ADSP-2181 EZ-KIT Lite

The *VisualDSP++ User's Guide for ADSP-21xx DSPs* contains most of the information you need to operate the VisualDSP++ debugger with your EZ-KIT Lite evaluation board. Because the manual was written using a simulator as a target, there are some differences and restrictions in the debugger operation when connected to a hardware target that are described in this section.

4.2.1.1 Loading Programs

Because you are loading programs into a hardware target, the load process takes slightly more time then loading in the simulator. Wait for the Load Complete message in the Output window before you perform any debug activities.

To load a program:

1. From the File menu, select Load.

   The Open a Processor Program dialog box appears.

2. Navigate to the folder where your DSP executable file resides.

   The demos that are supplied with the EZ-KIT Lite are located in <installation path>. An example default path is:
   `C:\Program Files\Analog Devices\VisualDSP\218x\EZ-KITs\2181\Examples.`

3. Select the file and click Open.

   The file loads and the message "Load Complete" appears in the Output window when the

load process has completed.

4.2.1.2 Registers and Memory

To see current values in registers and memory, use the F12 key or the Window Refresh command.

⃠ Register and memory contents may not be changed while a user program is running.

4.2.1.3 Setting Breakpoints and Stepping

⃠ Breakpoints set in the last three instructions of a DO-loop are allowed but this causes improper debugger operation.

ⓘ The debugger automatically inserts breakpoints at the function Main(), when the Settings Run To Main command is checked, and at the _exit instruction.

4.2.1.4 Resetting the EZ-KIT Lite Board

The EZ-KIT Lite board can be reset with the push button switch on the board or with the Debug Reset command from the debugger. After performing a reset, reload any programs you were running. The Debug Restart command also resets the processor. However, the processor retains all debug information and memory contents.

ⓘ The following sequence must be used when starting the debugger:

1. Start the debugger from the Windows Start menu.

   The debugger starts and the target message “Hit Reset Button” appears.

2. Press the Reset button.

3. Click OK.

⃠ Do not use the Reset button while the debugger is open, unless the debugger requests you to press it.

4.3 Demonstration Programs

The demos included with the EZ-KIT Lite are designed to show you the features and capabilities of the ADSP-2181 DSP. The demos are listed by the executable file name and are described by their output. The demos are located in <installation path>. An example default path is: `C:\Program Files\Analog Devices\VisualDSP\218x\EZ-KITs\2181\Examples.`

⃠ Do not run more than one ADSP-2181 EZ-KIT Lite session in the debugger at any one time. You may run an EZ-KIT Lite session and a simulator or ICE session at the same time, or you can open two debugger interfaces to run more than one EZ-KIT Lite session.

4.3.1 ADPCM.dxe

This program demonstrates Adaptive Differential Pulse Code Modulation (ADPCM) capabilities. ADPCM consists of a number of real-time speech compression algorithms.

4.3.2 DTMF.dxe

This demonstration generates Dual-Tone Multi-Frequency (DTMF) tones, as used in the telephone network for pushbutton signaling. A DTMF tone is composed of two different single frequency tones, one of four row tones added to one of four column tones. Thus, a full implementation of a DTMF standard tone generator can generate 16 different tones (only 12 are commonly used on consumer handsets).

4.3.3 ECHO.dxe

This demonstration uses the codec to generate an echo and the four-channel DAC to display the taps of the echo canceller.

4.3.4 Primes.dxe

This demonstration is a C program that generates the first 20 prime numbers.

4.3.5 FIRDEMO.dxe

This demonstration starts with a talk-through program. The AD1847 codec digitizes the analog microphone input and transmits the data to the DSP's serial port. The DSP reads data from the serial port and re-transmits the data back to the codec. The codec converts the data to an analog signal that drives the speaker. No digital signal processing is performed on the data. When you speak into the microphone, you should hear your voice through the speaker.

The filters have equivalent bandwidth and are evenly spaced on a logarithmic frequency axis. All FIR filters are 256 taps, and have been designed for 0.1 ripple.

FIR	*Filter*	*Lower Stop Band Pass Band*	*Upper Stop Band*
FIR1	0 - 269 Hz	328 - 448 Hz	547 - 4000 Hz
FIR2	0 - 426 Hz	521 - 710 Hz	866 - 4000 Hz
FIR3	0 - 675 Hz	825 - 1125 Hz	1375 - 4000 Hz
FIR4	0 - 1070 Hz	1308 - 1783 Hz	2179 - 4000 Hz

4.3.6 LPC2K4.dxe

Push the Interrupt button on EZ-KIT Lite to toggle between talk through and 2.4K LPC encoding. The red LED will light up when LPC encoding is in effect.

4.3.7 LPC7K8.dxe

Push the Interrupt button on EZ-KIT Lite to toggle between talk through and 7.8K LPC encoding. The red LED will light up when LPC encoding is in effect.

5 WORKING WITH EZ-KIT LITE HARDWARE

5.1 Overview

This chapter discusses hardware design issues on the ADSP-2181 EZ-KIT Lite board. The EZ-KIT Lite board schematics are available as an insert at the end of this manual.

5.2 EZ-KIT Lite Specifications

Processor:	ADSP-2181KS-133 operating at an instruction rate of 33 MHz (16.667 external clock)
Analog interface:	AD1847 stereo codec
Analog inputs:	One stereo pair of 2V RMS AC-coupled line level inputs One stereo pair of 20mV RMS AC-coupled microphone inputs
Analog outputs:	One stereo pair of 1V RMS AC-coupled line level outputs
Power source:	8 to 10V DC at 300mA
Environment:	0 to 70° Centigrade; 10 to 90 percent relative humidity (non-condensing)

5.3 System Architecture

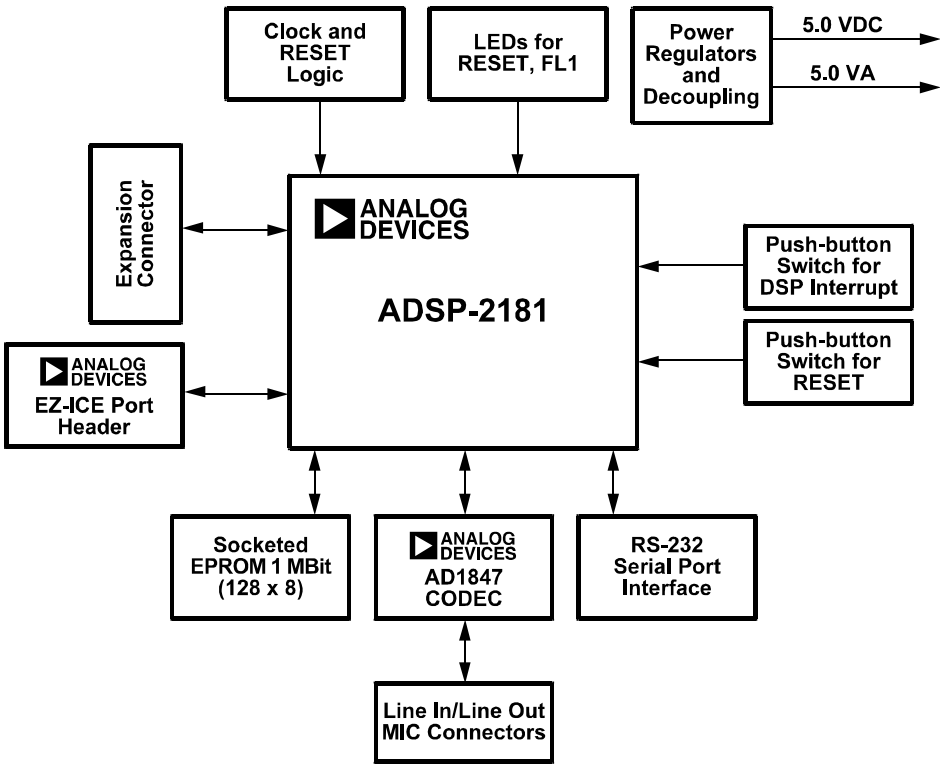


Figure 5-1 EZ-KIT Lite System Block Diagram

5.4 Board Layout

Figure 5-2 shows the layout of the EZ-KIT Lite board. This figure highlights the locations of the major components and connectors. Each of these major components is described in the following sections.

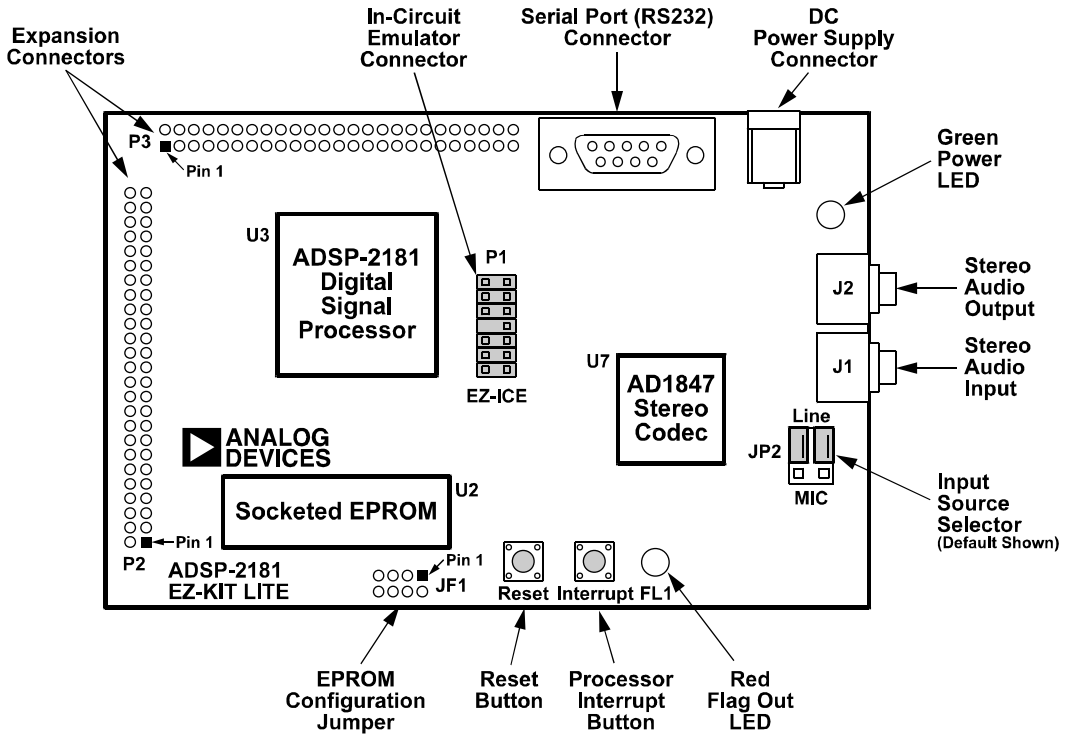


Figure 5-2 EZ-KIT Lite Board Layout

5.4.1 Socketed Memory

The socketed EPROM provides up to 128K x 8 bits of program storage that can be loaded by the ADSP-2181 when the DSP is programmed to boot from the socketed EPROM. After the ADSP-2181 is reset, the BDMA feature is used to load the first 32 words of program memory from byte memory space. Program execution is held off until all 32 words are loaded. Refer to the appropriate processor's Family User's Manual and the ADSP-2181 data sheet for more information on program booting and processor modes.

5.4.2 User LEDs

D1 is a red light emitting diode, which is controlled by the FL1 output of the ADSP-2181 processor. Software can control the state of this indicator by writing to an internal register.

D2 is a green light emitting diode, which is on whenever the board has power.

5.4.3 Switches

S1 is the reset pushbutton switch. Pushing this button causes the ADSP-2181 processor and the AD1847 codec to enter the hardware reset state and remain there until it is released.
The switch outputs are de-bounced electronically to prevent multiple transitions due to mechanical contact bounce.

S2 is the interrupt pushbutton switch. Pushing this button causes the ADSP-2181 to receive an $\overline{\text{IRQE}}$ interrupt input. The processor then executes the current $\overline{\text{IRQE}}$ interrupt handler software if the interrupt is enabled and the $\overline{\text{IRQE}}$ interrupt vector is in place. The interrupt switch output is de-bounced electronically to prevent multiple interrupts due to mechanical contact bounce.

5.4.4 Power Connector

The power connector supplies DC voltages to the EZ-KIT Lite board. Table 5-1 shows the power connector pin-out. If you do not use the power supply provided with your EZ-KIT Lite board, replace it with one that has the connections shown in Table 5-1.

Table 5-1 Power Connection

Terminal	Connection
Center pin	8 – 10v DC @ 300mA
Outer Ring	positive

5.4.5 European Power Supply Specifications

Table 5-2 European Power Supply Specifications

DC VOLTAGE:	8 to 10V DC
CURRENT:	300mA
DC CONNECTOR:	
Type:	Switchcraft 760 style, FEMALE
Plug Size:	5.5 (OD) X 2.1 (ID) X 12 (length) millimeters
Polarity:	Center is Negative (inside terminal)

5.4.6 AD1847 Connections

When the AD1847 is enabled, you can access the audio input and output jacks on the board. Each of the audio connectors are stereo mini jacks and accept standard commercially available stereo mini plugs.

The Microphone/Line_in input jack connects to the LINE_IN_L (left) and LINE_IN_R (right) pins or the MIC1 and MIC2 of the AD1847 SoundPort Stereo codec, depending on the setting of jumpers JP2. For more information, see the connections descriptions.

The LINE Output jack connects to the left (L) LINE_OUT and right (R) LINE_OUT pins of the codec.

5.4.7 Expansion Port Connectors

The two expansion port connectors provide access to the bus signals of the ADSP-2181. One possibility for the use of these connectors, beyond debugging, is host control. All interrupts, bus signals, and PWM event signals are available through this port. For more information, see "Expansion Connectors".

⃠ WARNING: External port loading can effect external bus speed and performance.

5.4.8 Connectors and Headers

J1 is a 1/8 inch (3.5 mm) stereo jack. This jack is used to bring line level or microphone audio signals into the board.

J2 is a 1/8 inch (3.5 mm) stereo jack. This jack is used to bring out line level audio signals from the board.

J3 is a female 9-pin D-Sub connector. It is used to communicate with a host computer using RS-232 signal levels and asynchronous serial protocols.

J4 is a jack for a 5.5 mm cylindrical plug. It is used to supply power to the board. The center pin of the jack is 2 mm diameter and should connect to the negative side of the power source. The outer sleeve of the mating plug must be positive.

JP1 is a site for an eight-pin header. It can be used to configure the board for EPROM sizes other than the 1 Mbit (128K byte) EPROM (27C010) shipped with the board. Most users will not need this feature. For more information see section on EPROM Jumper Settings.

JP2, shown in figure 5-3, is a six-pin header. It is used to configure input jack J1 for line level or microphone input. The center pin in each group of three is connected to one of the AD1847 codec's input pins. Jumpers (also known as shunts or shorting links) can be used to connect these pins to the output of the microphone amplifier or to the output of the line level input filter.

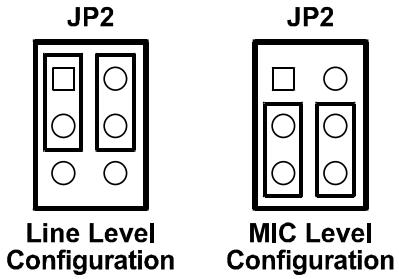


Figure 5-3 JP2 Jumper Settings

P1 is a 14-pin header connector used to connect to an ADSP-218x EZ-ICE® in-circuit emulator. Pin 7 should be removed for keying purposes. For more information, see " EZ-ICE Connector".

P2 and P3 are sites for 50-pin header connectors. These connectors can be used to access the ADSP-2181 signals for expansion or test purposes. For more information, see " Expansion Connectors".

U2 is a socket for an EPROM in a DIP package. As built the board will accept a 27C512 (64K byte) or 27C010 (128K byte) EPROM. Changing connections at JP1 allows the board to accept a 27C256 (32K byte), 27C020 (256K byte), 27C040 (512K byte), or 27C080 (1 Mbyte) EPROM. This socket is connected to the ADSP-2181's byte-wide memory interface.

R28 is a site for a zero ohm resistor. It this resistor is installed the ADSP-2181 processor can reset the board under software control. The software would assert reset by configuring PF0 as an output and then setting it low.

R29 is another site for a zero ohm resistor. If this resistor is installed and X3 and C37 are removed the codec can operate off of the ADSP-2181's CLKOUT signal instead of its own 24.576 MHz clock. It will also be necessary to change X1 to a lower frequency value to stay within the codec's ratings.

5.4.9 EPROM Jumper Settings

JP1 allows the ADSP-2181 EZ-KIT Lite board to be configured for any one of six different EPROM sizes. As shipped the board can accommodate either a 21C512 or 27C010. If some other size EPROM is installed in the socket at U2 it will be necessary to change the connections at JP1 shown in figure 5-4.

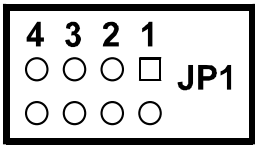


Figure 5-4 JP1 Jumper Settings

Connections are made vertically between pads. The pair of pads below each number constitutes the jumper position associated with that number. Connections can be made in several ways. If an eight-pin header is installed and the etch connections on the back are cut, EPROM size changes can be accommodated easily by installing and removing shunts. If frequent size changes are not contemplated, it may be sufficient to solder wires between the pads and so make the connections permanent.

Connections for 27C256 EPROM should look like figure 5-5.

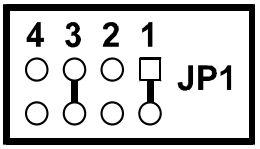


Figure 5-5 JP1 Jumper Setting for 27C256 EPROM

Note: This involves cutting the etch on the back of the board at jumper position 2 and adding a connection at jumper position 1.

Connections for a 21C512 or 27C010 EPROM should look like figure 5-6.

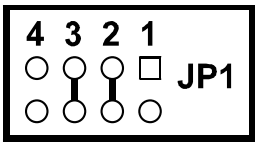


Figure 5-6 JP1 Jumper Settings for 21C512/27C010 EPROM

Note: This is how the connections are arranged when the board is manufactured.

The connections for a 27C020, 27C040, or 27C080 EPROM should look like figure 5-7.

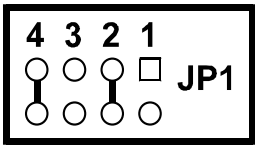


Figure 5-7 JP1 Jumper Settings for 27C020/27C040/ 27C080 EPROM

Note: This involves cutting the etch on the back of the board at jumper position 3 and adding a connection at jumper position 4.

5.4.10 Hardware Operation

When power is applied to the board, the reset circuit holds the processor in reset for approximately 30 ms. Reset is then deasserted and the processor begins the boot process. The BMODE and MMAP pins on the ADSP-2181 are grounded so the processor boots from the byte memory interface, which is connected to the EPROM socket. If the EPROM supplied with the board is installed in the socket, the operation of the board will proceed as documented in the software section of this manual.

5.4.11 EZ-ICE Connector

The ADSP-218x EZ-ICE® Emulator aids in the hardware debugging of an ADSP-2181 system. The emulator consists of hardware, host computer resident software, and the target board connector. The ADSP-2181 integrates on-chip emulation support with a 14-pin ICE-Port interface (Figure 5-3). This interface provides a simpler target board connection that requires fewer mechanical clearance considerations than other ADSP-2100 family EZ-ICEs. The ADSP-2181 device need not be removed from the target system when using the EZ-ICE, nor are any adapters needed. Due to the small footprint of the EZ-ICE connector, emulation can be supported in final board designs.

The EZ-ICE performs a full range of functions, including:

- In-target operation
- Up to 30 breakpoints
- Single-step or full-speed operation
- Registers and memory values can be examined and altered
- PC upload and download functions
- Instruction-level emulation of program booting and execution
- Complete assembly and disassembly of instructions
- C source-level debugging

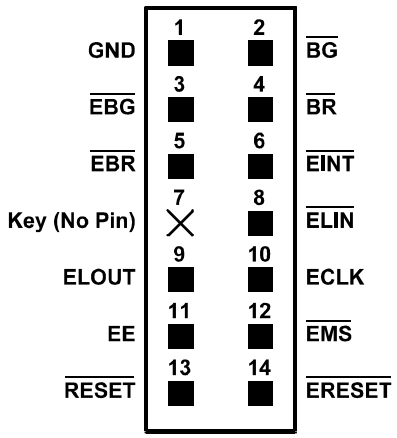


Figure 5-8 EZ-ICE 14-Pin Header (P6)

For more information on connecting to an ICE, see the ADSP-2181 data sheet and *Application Note EE-34*.

5.5 Designing an EZ-ICE Compatible Target

This section describes the ADSP-218x family EZ-ICE theory of operation to aid you in your design of a compatible target system.

The hardware consists of a printed circuit board measuring 3.5 inches by 5.5 inches. Assembled onto the printed circuit board are an ADSP-2181 digital signal processor, a socketed EPROM, an AD1847 codec, and various support circuits and connectors. The board is a complete signal processing system designed to demonstrate the capabilities of the ADSP-2181 digital signal processor. It can also be used as a platform to develop new applications for the ADSP-2181.

The EZ-KIT Lite board is an example of a minimum implementation of an ADSP-2181 processor. The socketed EPROM is connected to the processor via the Byte DMA port. This interface uses only eight of the twenty-four data lines to carry data (D8 through D15). Eight of the spare data lines (D16 through D23) are used to provide additional address bits. This allows the ADSP-2181 to address up to 32 Mbits (4 Mbytes) of memory. The DSP is configured to boot from the socketed EPROM when $\overline{\text{RESET}}$ is de-asserted or if power is applied to the board.

The AD1847 codec is connected to the DSP via SPORT0. This high-speed synchronous serial port carries all of the data, control, and status information between the DSP and the codec. It is possible to disable the codec if the serial port is to be used for another purpose. The CODECDIS signal available on connector P3 can be used to disable the codec. When this signal is brought low, the codec is disabled and its signals are put in a high-impedance state.

The SPORT1 pins are used to communicate with the host PC via the RS-232 interface (J3). The Flag In and Flag Out pins carry the receive and transmit data. Software running on the DSP emulates a UART to provide the proper protocol for asynchronous serial communications up to a data rate of 115K bits per second.

5.5.1 Hardware Debugging

If the green LED fails to light, check your power connections. Verify that your power supply has the proper size connector and that the polarity is correct. The power supply voltage measured at the connector to the board should be 8V to 10V DC. Also, ensure that there are no objects beneath or on top of the board that may cause a short circuit. Press the reset button (S1) if the board appears to be operating improperly.

5.6 Expansion Connectors

The two expansion connectors provide access to the ADSP-2181's interface pins. These pins let you watch data transmissions. In addition, the host interface, interrupt, and pwm_event pins are also available on this connector.

P2 and P3 are sites for 50-pin header connectors. These connectors can be used to access the ADSP-2181 signals for expansion or test purposes. The pin numbers on these connectors are arranged as follows.

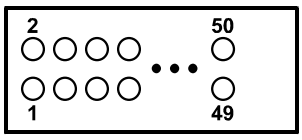


Figure 5-9 Expansion Connector

The signals available on these pins are shown in Table 5-3.

Table 5-3 ADSP-2181 Pin Names

P2				P3			
Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name	Pin #	Signal Name
1	A0	2	A1	1	GND	2	IAD0
3	A2	4	A3	3	IAD1	4	IAD2
5	A4	6	A5	5	IAD3	6	IAD4
7	A6	8	A7	7	IAD5	8	IAD6
9	A8	10	A9	9	IAD7	10	IAD8
11	A10	12	A11	11	IAD9	12	IAD10
13	A12	14	A13	13	IAD11	14	IAD12
15	D0	16	D1	15	IAD13	16	IAD14
17	D2	18	D3	17	IAD15	18	GND
19	D4	20	D5	19	$\overline{\text{IACK}}$	20	IAL
21	D6	22	D7	21	$\overline{\text{IS}}$	22	$\overline{\text{IWR}}$
23	D8	24	D9	23	$\overline{\text{IRD}}$	24	GND
25	D10	26	D11	25	PF0	26	PF1
27	D12	28	D13	27	PF2	28	PF3
29	D14	30	D15	29	PR4	30	PF5
31	D16	32	D17	31	PF6	32	PF7
33	D18	34	D19	33	FL0	34	FL1
35	D20	36	D21	35	FL2	36	CLKOUT
37	D22	38	D23	37	$\overline{\text{RESET}}$	38	$\overline{\text{IRQL0}}$
39	$\overline{\text{WR}}$	40	$\overline{\text{RD}}$	39	IRQL1	40	$\overline{\text{IRQ2}}$
41	$\overline{\text{IOMS}}$	42	$\overline{\text{BMS}}$	41	$\overline{\text{PWD}}$	42	PWDACK
43	$\overline{\text{DMS}}$	44	$\overline{\text{CMS}}$	43	$\overline{\text{CODECDIS}}$	44	TXD0
45	$\overline{\text{PMS}}$	46	$\overline{\text{BR}}$	45	TFS0	46	RFS0
47	$\overline{\text{BGH}}$	48	$\overline{\text{BG}}$	47	RXD0	48	SCK0
49	VCC	50	GND	49	VCC	50	GND

APPENDIX A RESTRICTIONS

APPENDIX B Restrictions

The following restrictions apply to release 1.1 of the ADSP-2181 EZ-KIT Lite evaluation board. For information on the ADSP-2181 silicon anomalies, visit the Web site at: http://www.analog.com/technology/dsp/EZAnswers/anomalies/index.html.

1. Breakpoints set in the last three instructions of a DO-loop are allowed, but cause your code to run incorrectly.

2. The host loses contact with the monitor while the user program is running if the user program disables the Timer interrupt or changes the Timer interrupt vector.

3. The host loses contact with the monitor while the program is running and in an ISR when nesting is turned on.

4. Do not use the reset button while the debugger is open unless the debugger requests you to. This causes the debugger to stop communicating.

5. Do not run more than one ADSP-2181 EZ-KIT Lite session in the debugger at any one time. You may run an EZ-KIT Lite session and a simulator or ICE session at the same time, or you can open two debugger interfaces to run more than one EZ-KIT Lite session.

APPENDIX C BILL OF MATERIALS

The following is a list of the components that are supplied on the EZ-KIT Lite evaluation board.

ITEM	QTY	DESC	PART NO	BOARD REF NO
1	1	Jack, Power	DJ005A	J4
2	1	Jack, Stereo GND	J-353-1000	J1
3	1	Jack, Stereo	J-353-103	J2
4	2	Push Button, N.O.(Thru-hole)	EVQPAC04M	S1, S2
5	20	Capacitor 1206 0.1uF	MCH315C104M	C1 C3 C6-C11 C24-C28 C33 C38 C39 C42-C45
6	7	Capacitor 1206 0.33uF	MCH312C334M	C2 C12 C17 C19 C22 C29 C34
7	6	Capacitor 1206 18pF	MCH315A180J	C4 C5 C31 C32 C36 C37
8	2	Capacitor 1206 220pF	MCH315SL221K	C14 C21
9	2	Capacitor 1206 560pF	MCH315SL561K	C13 C23
10	7	Capacitor, Aluminum 1.0uF SMT	CB1/50BM	C15 C16 C18 C20 C35 C40 C41
11	3	Capacitor, Aluminum 10uF SMT	CB10/16BM	C30 C46 C47
12	1	Connector, DB9 Female	DDFEX	J3
13	1	Crystal 16.67MHz	ABL-16.667MHZ	X1
14	1	Crystal 16.9344MHz	ABL-16.9344MHZ	X2
15	1	Crystal 24.576MHz	ABL-24.576MHZ	X3
16	1	DIODE	SMB4001	D3
17	1	1 Mbit EPROM	MX27C010DC-20	U2
18	1	Ferrite Bead 125 Ohm @ 100MHz	BCB-1812	FB1
19	1	Header, SQ. Pin 2x7	TSW-107-07-T-D	P1
20	1	Header, SQ. Pin 2x3	TSW-103-07-T-Q	JP2
21	1	LED, Green 5mm	LN31GPHL	D2
22	1	LED, Red 5mm	LN21RPHL	D1
23	1	IC, CODEC	AD1847JP	U7
24	1	IC, DSP	ADSP2181KS	U3
25	1	IC, Hex inverter	MC74HC14AD	U1
26	1	IC, Dual OPAMP	SSM2135S	U4
27	1	IC, Regulator 5 Volt TO-220	LM78M05CT	U6
28	1	IC, RS-232 Interface	ADM232AARN	U5
29	1	PCB, ESDSP-81	65-000286-01	
30	3	Resistor, 1/8W 5% 1206 100K	MCR18-EZHU-J-104	R1 R3 R18
31	9	Resistor, 1/8W 5% 1206 10K	MCR18-EZHU-J-103	R20-R27 R5
32	2	Resistor, 1/8W 5% 1206 240K	MCR18-EZHU-J-244	R14 R9
33	2	Resistor, 1/8W 5% 1206 270	MCR18-EZHU-J-271	R17 R6
34	2	Resistor, 1/8W 5% 1206 2K	MCR18-EZHU-J-202	R2 R4
35	2	Resistor, 1/8W 5% 1206 47K	MCR18-EZHU-J-473	R11 R13
36	6	Resistor, 1/8W 5% 1206 5.1K	MCR18-EZHU-J-512	R10 R12 R15 R16 R7 R8
37	1	Resistor, 1/8W 5% 1206 1.6	MCR18-EZHU-K-1R6	R19
38	4	Rubber bumper, gray	SJ-5018924157-R	
39	2	Shunt		On header at JP2
40	1	Socket, 32 Pin Dip	2-644018-5	U2

APPENDIX A SCHEMATICS

Revision	Date	Description	Approval
A		Initial Release	

Contents:

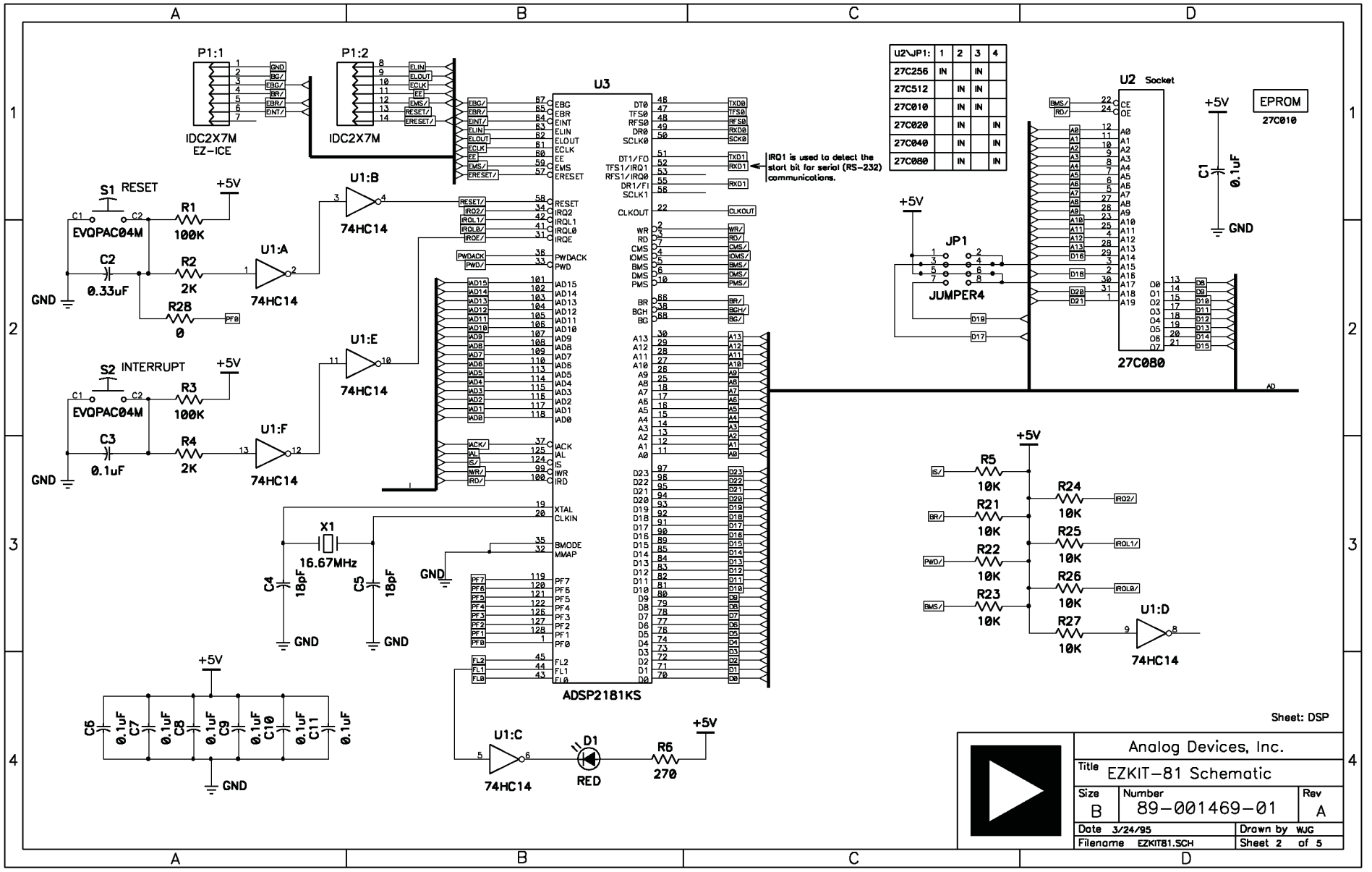
Sheet: Title

Analog Devices, Inc.

Title: EZKIT-81 Schematic

Size	Number	Rev
B	89-001469-01	A

Date 3/24/95	Drawn by WJG
Filename EZKIT81.SCH	Sheet 1 of 5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IDC2X7M
EZ-ICE
P1:2
IDC2X7M
U3
ADSP2181KS
U2 Socket
27C080
EPROM
27C010
JP1
JUMPER4
U2\JP1: 1 2 3 4
27C256 IN IN
27C512 IN IN
27C010 IN IN
27C020 IN IN
27C040 IN IN
27C080 IN IN
IRQ1 is used to detect the start bit for serial (RS-232) communications.
S1 RESET
S2 INTERRUPT
EVQPAC04M
R1 100K
R2 2K
R3 100K
R4 2K
R28 0
C1 0.1uF
C2 0.33uF
C3 0.1uF
U1:A
U1:B
U1:C
U1:D
U1:E
U1:F
74HC14
X1 16.67MHz
C4 18pF
C5 18pF
C6 0.1uF
C7 0.1uF
C8 0.1uF
C9 0.1uF
C10 0.1uF
C11 0.1uF
R5 10K
R21 10K
R22 10K
R23 10K
R24 10K
R25 10K
R26 10K
R27 10K
D1 RED
R6 270
+5V
GND
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Analog Devices, Inc.
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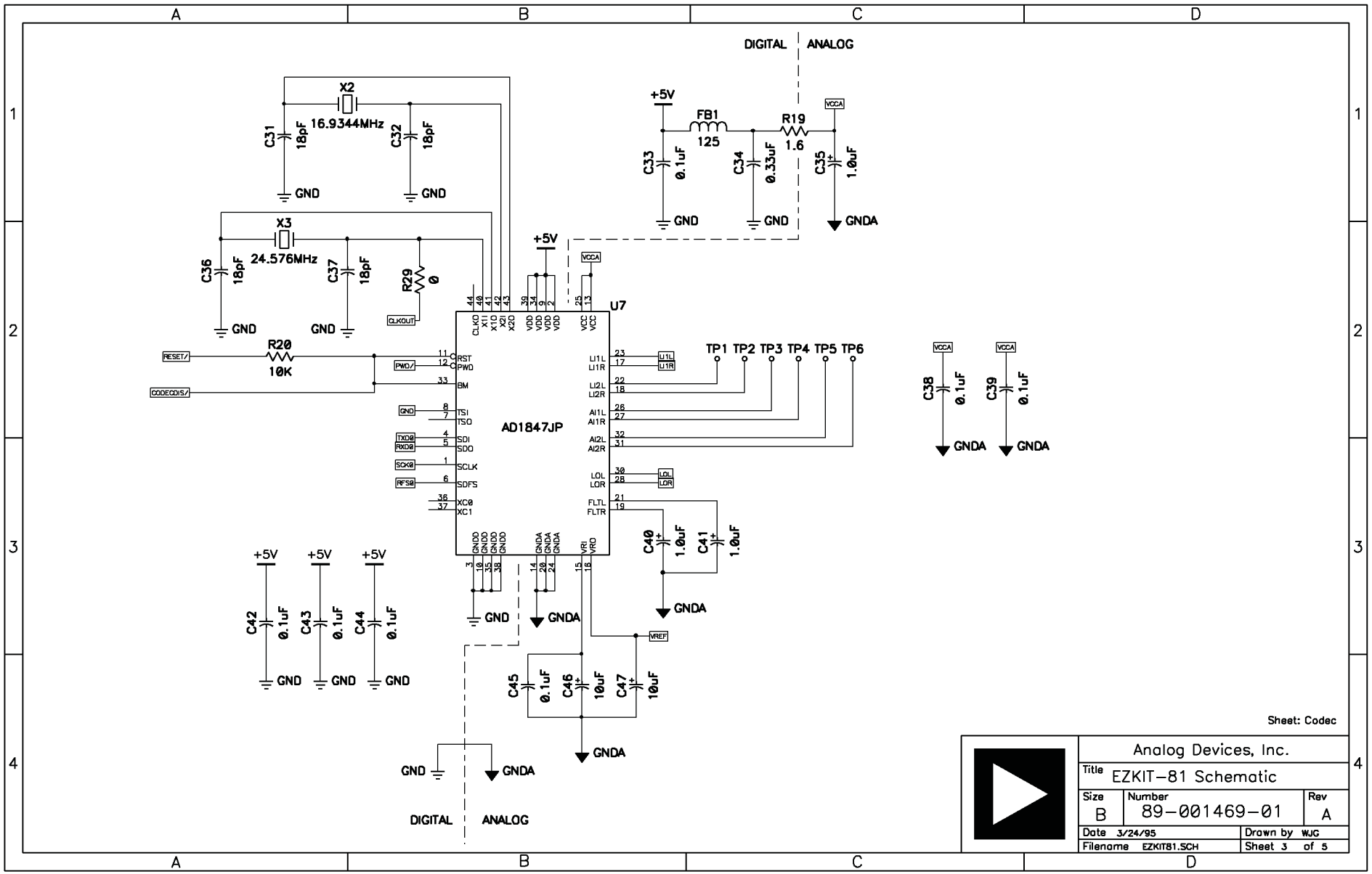
Size B
Number 89-001469-01
Rev A
Date 3/24/95
Drawn by WJG
Filename EZKIT81.SCH
Sheet 2 of 5


DIGITAL
ANALOG
X2
16.9344MHz
C31 18pF
C32 18pF
GND
X3
24.576MHz
C36 18pF
C37 18pF
R29 0
CLKOUT
+5V
FB1 125
R19 1.6
VCCA
C33 0.1uF
C34 0.33uF
C35 1.0uF
GNDA
U7
R20 10K
RESET/
PWD/
CODECDIS/
AD1847JP
TP1 TP2 TP3 TP4 TP5 TP6
C38 0.1uF
C39 0.1uF
C40 1.0uF
C41 1.0uF
C42 0.1uF
C43 0.1uF
C44 0.1uF
C45 0.1uF
C46 10uF
C47 10uF
VREF
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Rev A
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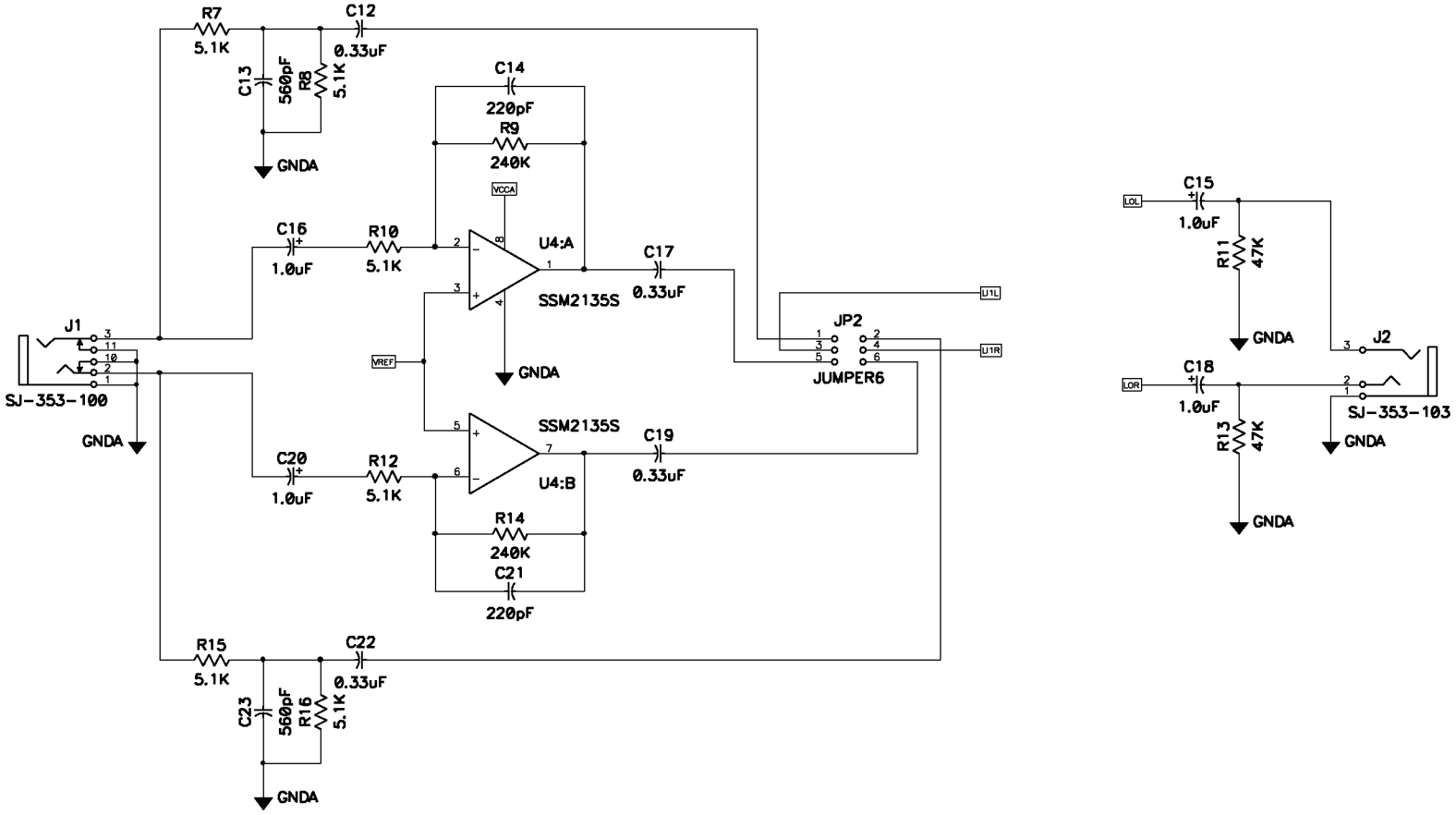
Drawn by WJG
Filename EZKIT81.SCH
Sheet 3 of 5



Sheet: Analog

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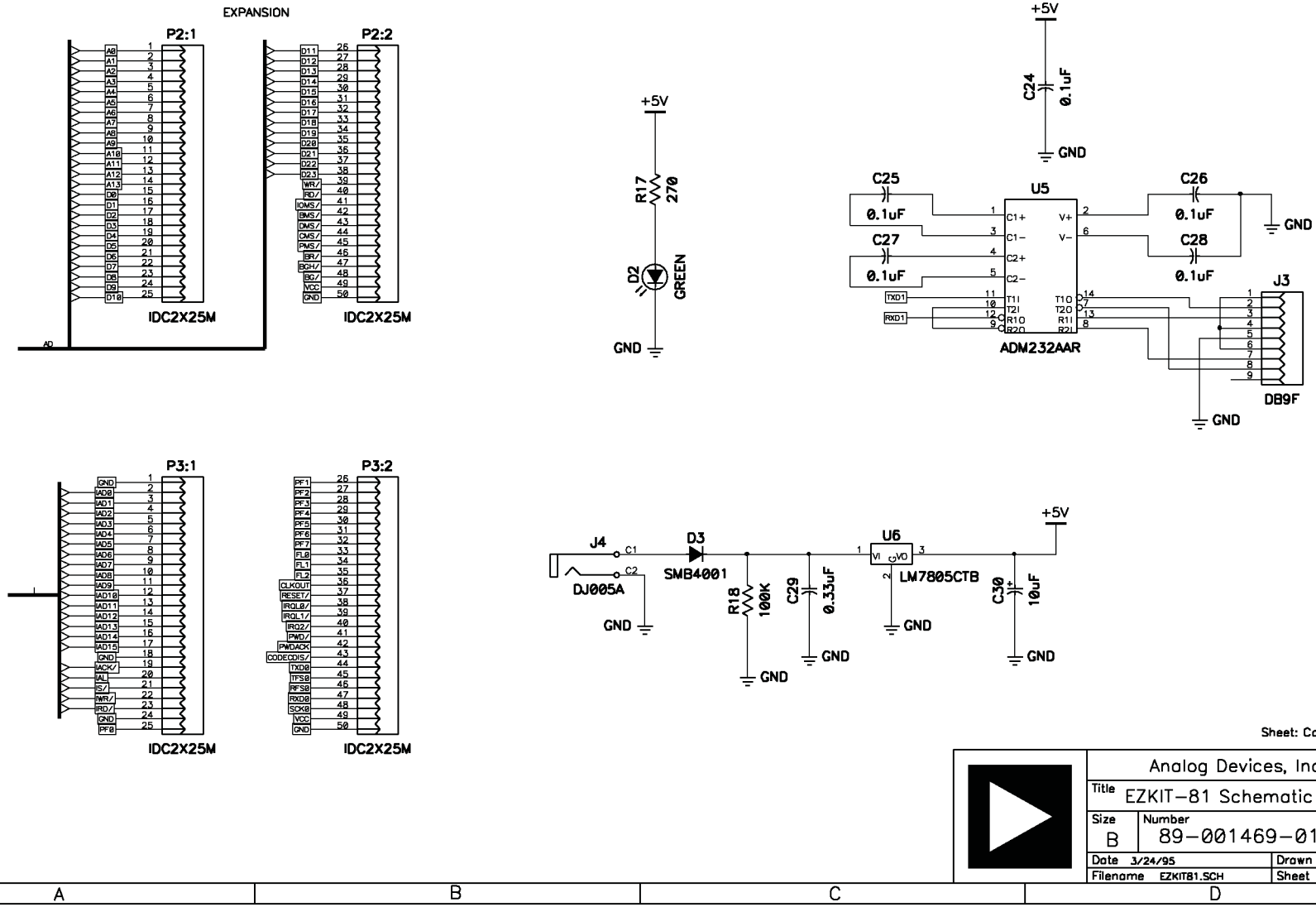
Filename: EZKIT81.SCH	Sheet 4 of 5	


EXPANSION
P2:1
P2:2
IDC2X25M
IDC2X25M
P3:1
P3:2
IDC2X25M
IDC2X25M
+5V
R17
270
D2
GREEN
GND
+5V
C24
0.1uF
GND
C25
0.1uF
C27
0.1uF
U5
C1+
C1−
C2+
C2−
V+
V−
T1I
T2I
R1O
R2O
T1O
T2O
R1I
R2I
ADM232AAR
C26
0.1uF
C28
0.1uF
GND
J3
DB9F
GND
TXD1
RXD1
J4
DJ005A
D3
SMB4001
R18
100K
C29
0.33uF
U6
LM7805CTB
C30
10uF
+5V
GND
GND
GND
GND
Sheet: Connectors
Analog Devices, Inc.
Title EZKIT−81 Schematic
Size B
Number 89−001469−01
Rev A
Date 3/24/95
Drawn by WJG
Filename EZKIT81.SCH
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